Amendments to the Specification:

Please replace the paragraph beginning at page 5, line 23, with the following rewritten paragraph:

In summary, previous fabrication schemes have relied upon litographically defined silicon channels and long, confined lateral epitaxial growth. However, a lithographically defined channel cannot be formed with sufficiently close tolerances and even ~~avalable~~ available tolerances cannot be maintained adequately to support near-optimal dual gate transistor performance in the above approaches. Further, techniques using lateral current flow with FET widths defined laterally suffer from difficulty in aligning the top and bottom gates even though thickness of silicon can be tightly controlled.

Please replace the paragraph beginning at page 12, line 23, with the following rewritten paragraph:

Figures 4A and 4B correspond to Figures 3A and 3B, respectively, after the etching of active layer ~~10~~ 110 and etch stop 202. If necessary, a trim mask can be applied to remove undesired fins 402 in accordance with conventional processing techniques widely known to those skilled in the art. Figure 5 shows the device of Figure 4A after the formation of a second channel 502 which, as will be readily recognized by those skilled in the art, can be formed by using the same processing steps as previously described ~~to~~ for the first channel 204.